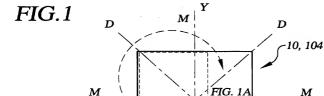
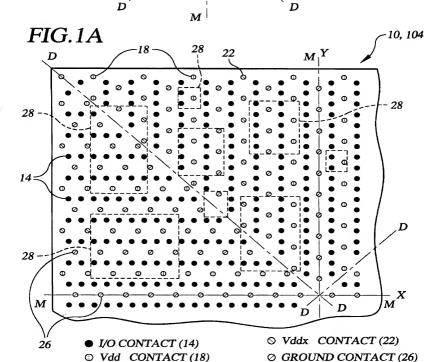
INTEGRATED CIRCUIT CHIP HAVING A RINGED WIRING LAYER INTERPOSED BETWEEN A CONTACT LAYER AND A WIRING GRID BEDNAR ET AL. BUR920020107US1 1/4





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FIG.2 PRIOR ART

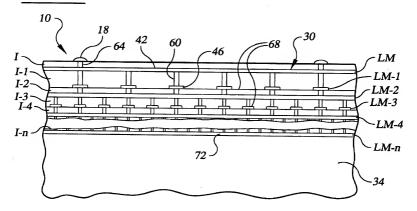
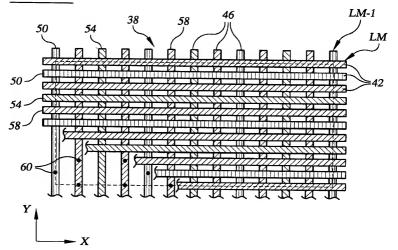
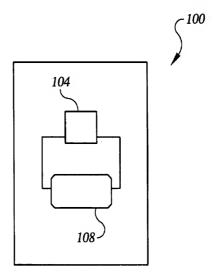


FIG.3
PRIOR ART

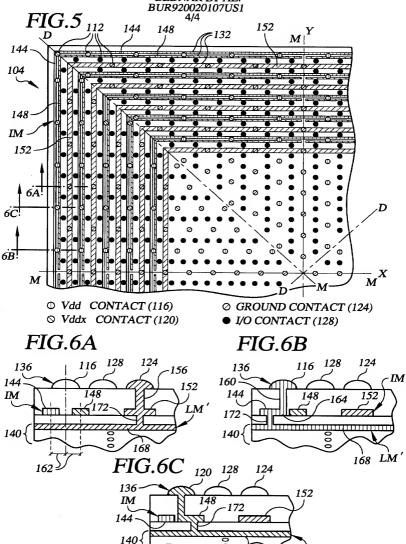


INTEGRATED CIRCUIT CHIP HAVING A RINGED WIRING LAYER INTERPOSED BETWEEN A CONTACT LAYER AND A WIRING GRID BEDNAR ET AL. BUR920020107US1 3/4

FIG.4



INTEGRATED CIRCUIT CHIP HAVING A RINGED WIRING LAYER INTERPOSED BETWEEN A CONTACT LAYER AND A WIRING GRID BEDNAR ET AL.



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